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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,092	05/23/2001	Mark Thomas McCormack	6136/54242 (25916-217)	5484
30764	7590	11/16/2005	EXAMINER	
SHEPPARD, MULLIN, RICHTER & HAMPTON LLP 333 SOUTH HOPE STREET 48TH FLOOR LOS ANGELES, CA 90071-1448			LEE, EUGENE	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/866,092	MCCORMACK ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 11 April 2005.
- 2a) ☐ This action is **FINAL**.      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 17-24, 26-34 and 36-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 17-24, 26-34 and 36-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/11/05 has been entered.

### ***Drawings***

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, (1) second integrated electronic component comprises a conductive contacting said second metallic layer (claim 28); (2) one metal-lined via extending **through** said metallic layer (claims 30-33); and (3) third dielectric layer disposed on said second side of said substrate (claim 44) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

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drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 28, and 44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

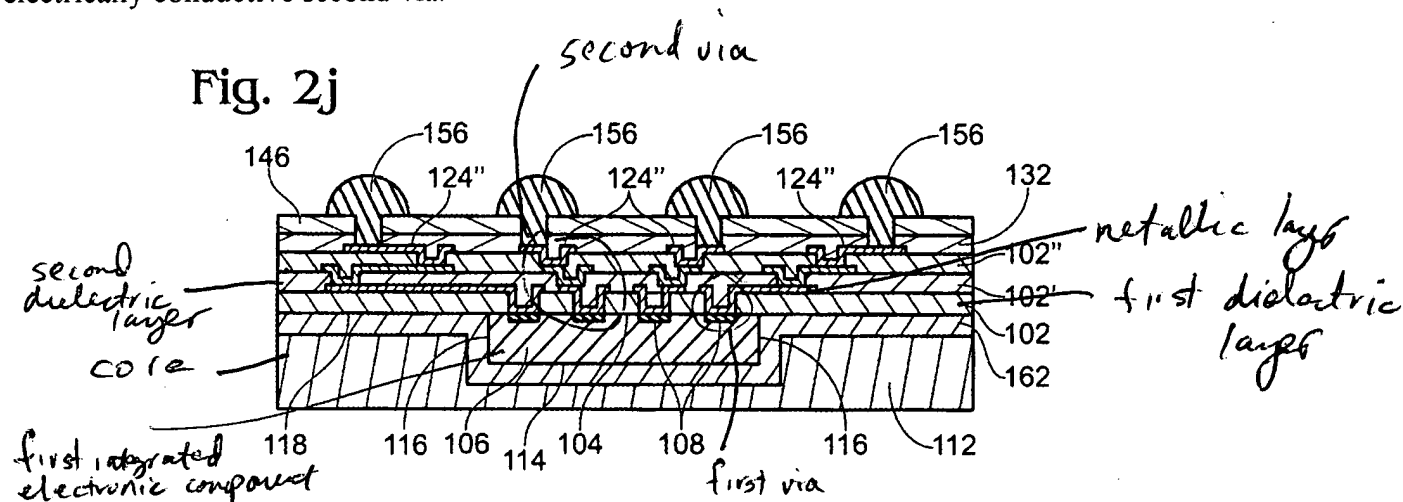
The specification does not describe a second integrated electronic component comprises a conductive contacting said second metallic layer (claim 28); and a third dielectric layer disposed on said second side of said substrate (claim 44).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 17, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. 6,154,366 in view of Saito et al. 5,049,980. Ma discloses (see, for example, Fig. 2j) a package (multi-layer printed circuit board) comprising an encapsulation material (circuit board substrate) 112 having a first substrate surface and a second substrate surface, die (first integrated electronic component) 106, cavity, flex component (first dielectric layer) 102, conductive trace (metallic layer) 124, electrically conductive first via, element (second dielectric layer) 102', and electrically conductive second via.



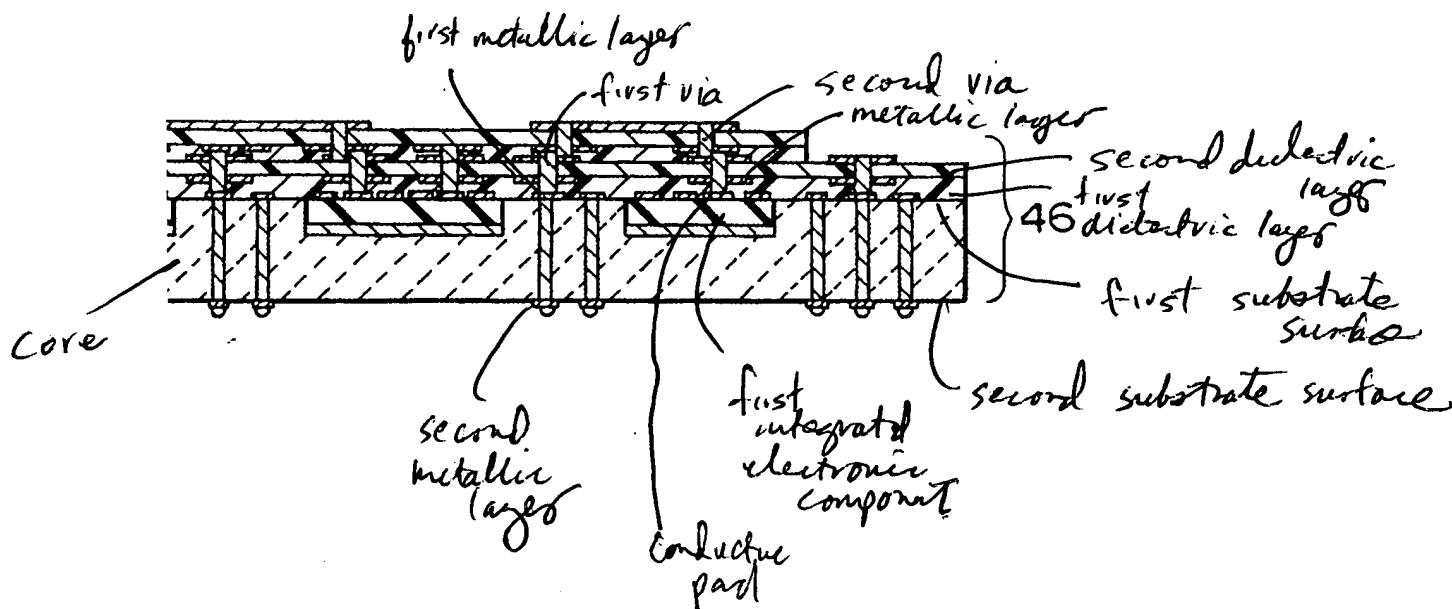
Ma does not disclose the circuit board substrate being polymeric. However, Saito discloses (see, for example, FIG. 5) an electronic circuit device comprising a semiconductor element 2, and resin substrate (circuit board substrate) 1. In column 2, lines 42-46, Saito discloses the resin substrate may be a polycarbonate resin, which is polymeric. Therefore, it would have been

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obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die, and any overlying layers.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Saito.

7. Claims 17, 18, 20 thru 23, 27, 30, 36, 38 thru 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. 5,565,706 in view of Saito et al. 5,049,980. Miura discloses (see, for example, FIG. 6) a multi-layer package board (multi-layer printed circuit board) comprising a package board (circuit board substrate) 46; ceramic substrate (core) 45 having a first substrate surface and a second substrate surface; LSI (first integrated electronic component) 35, spot facing portions (cavity) 37, adhesive sheet (first dielectric layer) 11, copper wiring (metallic layer) 9a, via (electrically conductive first via) 17, insulating layer (second dielectric layer) 9c, and via (electrically conductive second via) 16.



Miura does not disclose the circuit board substrate being polymeric. However, Saito discloses (see, for example, FIG. 5) an electronic circuit device comprising a semiconductor element 2, and resin substrate (circuit board substrate) 1. In column 2, lines 42-46, Saito discloses the resin substrate may be a polycarbonate resin, which is polymeric. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die, and any overlying layers.

Regarding claim 18, see figures wherein Miura discloses external output terminals (first metallic layer) 8 and external output terminals (second metallic layer) 28.

Regarding claim 27, see figures wherein Miura discloses external output terminals (conductive pad) 8 on top of the LSI 35.

Regarding claim 30, see FIG. 6 wherein Miura discloses one of the vias (at least one metal-lined via) 16 attached to LSI 33.

Regarding claim 36, see, for example, column 8, lines 25-28 wherein Miura discloses a capacitor.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Saito.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Desai 5,739,188. Miura in view of Saito does not disclose the

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multi-layer core substrate comprising at least two polymeric layers. However, Desai discloses (see, for example, column 3, lines 26-30) a multi-layered product wherein the product comprises a substrate layer/cap layer (two polymeric layers). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the multi-layer core substrate comprising at least two polymeric layers in order to protect the substrate.

9. Insofar as definite, claims 24, 26, 28, 29, 31, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Marcinkiewicz et al. 5,241,456. Miura in view of Saito does not disclose said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity. However, Marcinkiewicz discloses (see, for example, FIG. 1) a structure 10 comprising a substrate 12, and chip (second integrated electronic component) 36. Having the chip in the same substrate creates a multichip device that saves space and provides interconnection between two chips. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity in order to create a multichip device that saves space and provides interconnection between two chips.

Regarding claim 28, see, for example, FIG. 1 wherein Marcinkiewicz discloses contact pad (conductive pad) 38.



Regarding claim 29, see, for example, FIG. 1 wherein Miura discloses contact pad (conductive pad) 8 on top of the LSI 35.

Regarding claim 44, Miura in view of Saito does not disclose a third dielectric layer disposed on said second side of said substrate. However, Marcinkiewicz discloses (see, for example, FIG. 1) a substrate 12, and dielectric layer (third dielectric layer) 52. The dielectric layer protects the bottom surface of the substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a third dielectric layer disposed on said second side of said substrate in order to protect the bottom of the substrate.

10. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Ma et al. 6,154,366. Miura in view of Saito does not disclose additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer. However, Ma discloses (see, for example, FIG. 1d) a package comprising a die 106 and multiple conductive traces (at least one metal-lined via) 124. The multiple conductive traces transmit signals to the die. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have additionally at least one metal-lined via extending through said metallic layer and through said first dielectric layer in order to transmit more signals to the integrated electronic component.

11. Claims 37, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43,

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and 44 above, and further in view of Miyazawa et al. 5,953,619. Miura in view of Saito does not disclose said capacitor comprising a perovskite capacitance material. However, Miyazawa discloses (see, for example, column 1, lines 27-35) that a perovskite crystal structure has a high dielectric constant. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said capacitor comprising a perovskite capacitance material in order to have a higher dielectric constant in the same area.

### ***Response to Arguments***

12. Applicant's arguments with respect to claims 17-24, 26-34, and 36-44 have been considered but are moot in view of the new ground(s) of rejection.

### **INFORMATION ON HOW TO CONTACT THE USPTO**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee  
November 7, 2005

A handwritten signature in black ink, appearing to be 'Eugene Lee', with a stylized, flowing script.